YAO Lingyun

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Academic Background

11/2022-now	**Aalto University**	**Doctoral program in electrical engineering**
09/2020-06/2022	**Aalto University**	**Master program in Micro and nano-electronic circuit design**
09/2016-06/2020	**Central South University**	**Bachelor program in Microelectronics Science and Engineering**

Research Projects (Efficient hardware for Probabilistic AI)

- **AI chip for probabilistic AI inference acceleration (On going)**

  This work is developing a hardware accelerator to compute Probabilistic circuits (PCs) on-chip and integrate them in the sensor nodes. This chip will use innovative computation blocks and integrate the approximate computing method. Our chip will also support multiple models inference computing including NNs.

- **Approximate multipliers for Hardware-efficient Inference in Probabilistic Circuits (Whistle Project)**

  By using approximate "exp-sum-log" in hardware instead of "log-sum-exp" trick in software, our method obtains up to 357× and 649× energy reduction on custom hardware for evidence and MAP queries respectively with little or no computational error. It also brings less memory consumption and faster inference.

- **Probabilistic circuits (PCs) based self-adaptive RF transceiver (Whistle Project)**

  The RF transceiver has delay which can be tuned by parameter, yet this process is a Blackbox inside RF transceiver hardware. This work trained the parameters and the delay collected from an RF transceiver real data using PCs. The trained mode is implemented in FPGA, finally helping to achieve a self-calibrated RF transceiver.

- **Convolution encoder for low power wireless data flow (master project)**

  This work implemented convolution encoders based on different polynomials, compared the area, power, and bit error rate (BER) versus Eb/N0 over the QPSK channel, and evaluated configurations to improve the performance.

- **Electrochemical biosensors for cancer detection, Chip micro defects analysis, Chip thermoelectric coupling analysis (bachelor project)**

Internship Experience

Aalto Electronic circuit design group Research assistant (4/2021-06/2022)

- Using VHDL to describe PCs with different arithmetic methods, and different bits of numbers, and analysis the hardware accuracy. Building frameworks to automated transfer machine learning models to hardware. Improving the efficiency of hardware according to model, prepare for AI processors chip design.

Awards & grants

- HPY Research Foundation grant for the work: AI-based self-adaptive RF transceiver using hardware-efficient probabilistic models.
- Aalto university Dean Scholarship | Aalto university Full Admission Scholarship
- Second Prize of 2018-2019, Third Prize of 2016-2017, Third Prize of 2017-2018 academic year Scholarship of Central South University, National Encouragement Scholarship of China

Publications

- Leslin, Jelin, Antti Hyttinen, Karthekeyan Periasamy, Lingyun Yao, Martin Trapp, and Martin Andraud. "A Hardware Perspective to Evaluating Probabilistic Circuits." In International Conference on Probabilistic Graphical Models, pp. 349-360. PMLR, 2022.
- L Yao, M Trapp, K Periasamy, J Leslin, G Singh, M Andraud, Logarithm-approximate floating-point multiplier for hardware-efficient inference in probabilistic circuits, The 6th Workshop on Tractable Probabilistic Modeling, 2023.
- Yao, Lingyun, et al. "On Hardware-efficient Inference in Probabilistic Circuits." the 40th Conference on Uncertainty in Artificial Intelligence (UAI 2024).
- K Periasamy, J Leslin, A Korsman, L Yao, M Andraud, AutoPC: an open-source framework for efficient probabilistic reasoning on FPGA hardware, 2024 22nd IEEE Interregional NEWCAS Conference (NEWCAS), 2024.